IN THE CLAIMS

The following is a complete listing of the claims, and replaces all earlier versions and listings.

1. (Currently Amended) A data transfer circuit for transferring a data group having data represented by plural bits, without changing an arrangement of a sequence of the plural bits, from a first memory to a second memory for coding by a bit-plane coding processor, comprising:

detection means for detecting a maximum value in the data group as a transfer object, wherein the detecting processing by said detection means is performed while transferring the data group and completed before completion of the transfer; and

specifying means for specifying a non-zero highest-order bit position among bits constructing the maximum value detected by said detection means, and outputting a code representing the bit position specified by said specifying means to said bit-plane coding processor,

wherein a bit in a position higher than the highest-order bit position specified by said specifying means is omitted from coding executed by said bit-plane coding processor after transferring the data group to the second memory.

2. (Currently Amended) A data transfer circuit for transferring a data group having data represented by plural bits, without changing an arrangement of a sequence of

the plural bits, from a first memory to a second memory for coding by a bit-plane coding processor, comprising:

calculation means for performing a logical OR calculation independently for each bit-plane, each bit-plane comprising bits which are located at a same bit position among bits constructing data which all the data group has, wherein the processing of the logical OR calculation by said calculation means is performed while transferring the data group and completed before completion of the transfer; and

specifying means for specifying a non-zero highest-order bit position among bits constructing a result of the logical OR calculation by said calculation means, and outputting a code representing the bit position specified by said specifying means to said bit-plane coding processor,

wherein a bit in a position higher than the highest-order bit position specified by said specifying means is omitted from coding executed by said bit-plane coding processor after transferring the data group to the second memory.

3. (Currently Amended) A data transfer circuit for transferring a data group having data represented by plural bits, without changing an arrangement of a sequence of the plural bits, from a first memory to a second memory for coding by a bit-plane coding processor, comprising:

calculation means for performing a logical OR calculation independently for each bit-plane, each bit-plane comprising bits which are located at a same bit position among bits constructing data which all the data group has, wherein the

processing of the logical OR calculation by said calculation means is performed while transferring the data group and completed before completion of the transfer; and

specifying means for specifying a non-zero lowest-order bit position among bits constructing a result of the logical OR calculation by said calculation means, and outputting a code representing the bit position specified by said specifying means to said bit-plane coding processor,

wherein a bit in a position lower than the lowest-order bit position specified by said specifying means is omitted from coding by said bit-plane coding processor.

4. (Currently Amended) A data transfer circuit for transferring a data group having data represented by plural bits, without changing an arrangement of a sequence of the plural bits, from a first memory to a second memory for coding by a bit-plane coding processor, comprising:

calculation means for performing a logical OR calculation independently for each bit-plane, each bit-plane comprising bits which are located at a same bit position among bits constructing data which all the data group has, wherein the processing of the logical OR calculation by said calculation means is performed while transferring the data group and completed before completion of the transfer; and

specifying means for specifying a non-zero highest-order bit position and a non-zero lowest-order bit position among bits constructing a result of the logical OR

calculation by said calculation means, and outputting a code representing the bit position specified by said specifying means to said bit-plane coding processor,

wherein a bit in a position lower than the lowest-order bit position and a bit in a position higher than the highest-order bit position specified by said specifying means are omitted from coding by said bit-plane coding processor.

5. (Canceled)

6. (Previously Amended) The data transfer circuit according to claim 1, further comprising a DMA circuit.

7. (Previously Amended) The data transfer circuit according to claim 1, wherein the data group includes pixel data or transform coefficients generated by transform coding on the pixel data.

8. (Currently Amended) A data transfer method for transferring a data group having data represented by plural bits, without changing an arrangement of a sequence of the plural bits, from a first memory to a second memory for coding by a bit-plane coding processor, comprising:

a detection step, of detecting a maximum value in the data group as a transfer object, wherein the detecting processing in said detection step is performed while transferring the data group and completed before completion of the transfer; and

a specifying step, of specifying a non-zero highest-order bit position among bits constructing the maximum value detected in said detection step, and outputting a code representing the bit position specified in said specifying step to said bit-plane coding processor,

wherein a bit in a position higher than the highest-order bit position specified at said specifying step is omitted from coding executed by said bit-plane coding processor after transferring the data group to the second memory.

9. (Currently Amended) A data transfer method for transferring a data group having data represented by plural, without changing an arrangement of a sequence of the plural bits, bits from a first memory to a second memory for coding by a bit-plane coding processor, comprising:

a calculation step, of performing a logical OR calculation independently for each bit-plane, each bit-plane comprising bits which are located at a same bit position among bits constructing data which all the data group has, wherein the processing of the logical OR calculation in said calculation step is performed while transferring the data group and completed before completion of the transfer; and

a specifying step, of specifying a non-zero highest-order bit position among bits constructing a result of the logical OR calculation in said calculation step, and outputting a code representing the bit position specified in said specifying step to said bit-plane coding processor,

wherein a bit in a position higher than the highest-order bit position specified in said specifying step is omitted from coding by said bit-plane coding processor.

10. (Currently Amended) A data transfer method for transferring a data group having data represented by plural bits, without changing an arrangement of a sequence of the plural bits, from a first memory to a second memory for coding by a bit-plane coding processor, comprising:

a calculation step, of performing a logical OR calculation independently for each bit-plane, each bit-plane comprising bits which are located at a same bit position among bits constructing data which all the data group has, wherein the processing of the logical OR calculation in said calculation step is performed while transferring the data group and completed before completion of the transfer; and

a specifying step, of specifying a non-zero lowest-order bit position among bits constructing a result of the logical OR calculation in said calculation step, and outputting a code representing the bit position specified in said specifying step to said bit-plane coding processor,

wherein a bit in a position lower than the lowest-order bit position specified in said specifying step is omitted from coding by said bit-plane coding processor.

11. (Currently Amended) A data transfer method for transferring a data group having data represented by plural bits, without changing an arrangement of a

sequence of the plural bits, from a first memory to a second memory for coding by a bit-plane coding processor, comprising:

a calculation step, of performing a logical OR calculation independently for each bit-plane, each bit plane comprising bits which are located at a same bit position among bits constructing data which all the data group has, wherein the processing of the logical OR calculation in said calculation step is performed while transferring the data group and completed before completion of the transfer; and

a specifying step, of specifying a non-zero highest-order bit position and a non-zero lowest-order bit position among bits constructing a result of the logical OR calculation in said calculation step, and outputting a code representing the bit position specified in said specifying step to said bit-plane coding processor,

wherein a bit in a position lower than the lowest-order bit position and a bit in a position higher than the highest-order bit position specified in said specifying step are omitted from coding by said bit-plane coding processor.

12. (Original) The data transfer method according to claim 8, wherein said data transfer method includes a data transfer method in a DMA circuit.